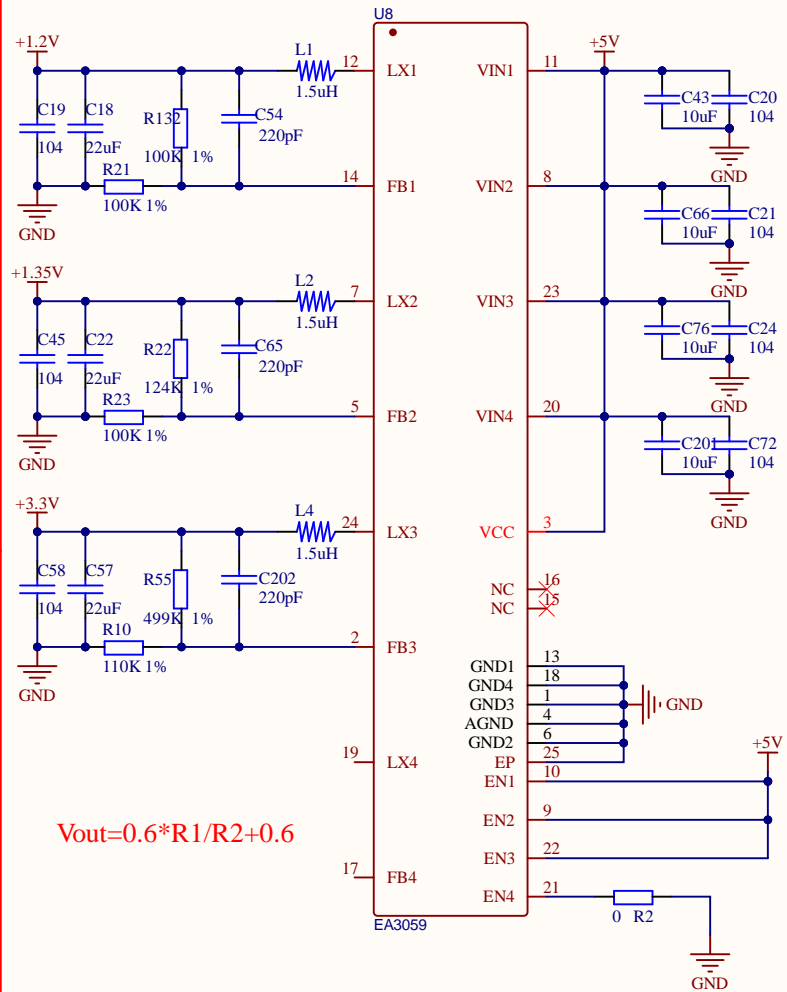
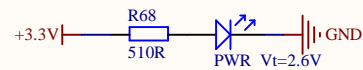


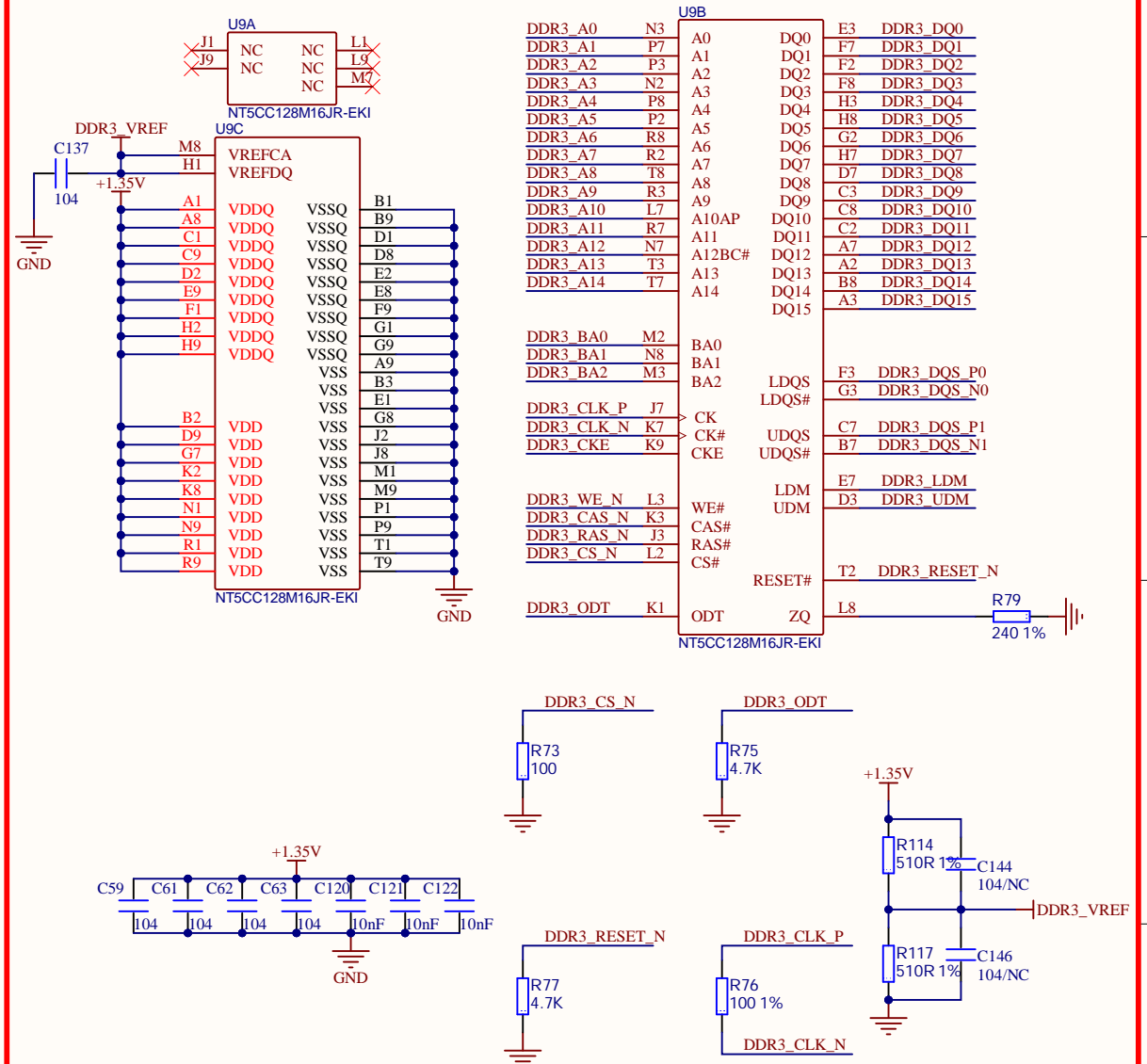
## POWER Chip



## 3.3V POWER



## DDR3

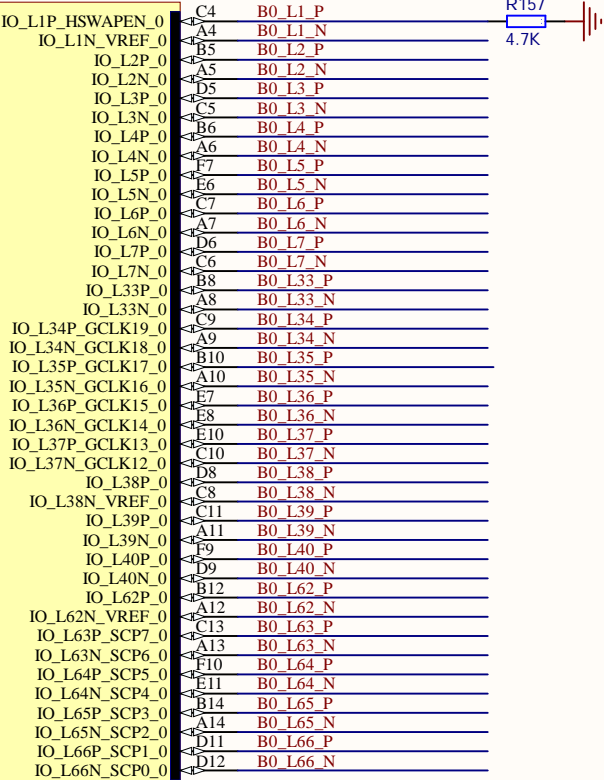


Title		
Size	Number	Revision
A4		
Date:	11/12/2024	Sheet of
File:	D:\01_rw\...\01_POWER&DDR_CORE.Sch	Drawn By:

FPGA BANK0

U16A

BANK 0

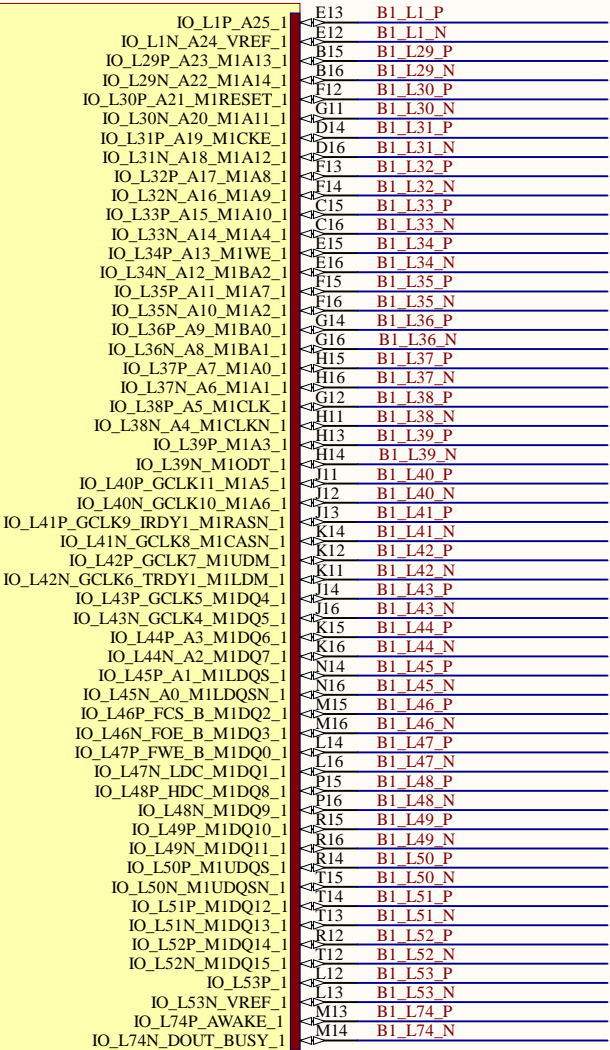


XC6SLX9/X16/X25-2FTG256I

FPGA BANK1

U16B

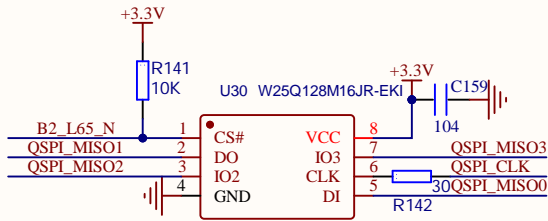
BANK 1



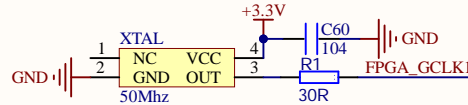
XC6SLX9/X16/X25-2FTG256I

Title		
Size	Number	Revision
A4		
Date:	11/12/2024	Sheet of
File:	D:\01_rw\...\02_FPGA_Bank0_Bank1.Sch	Drawn By:

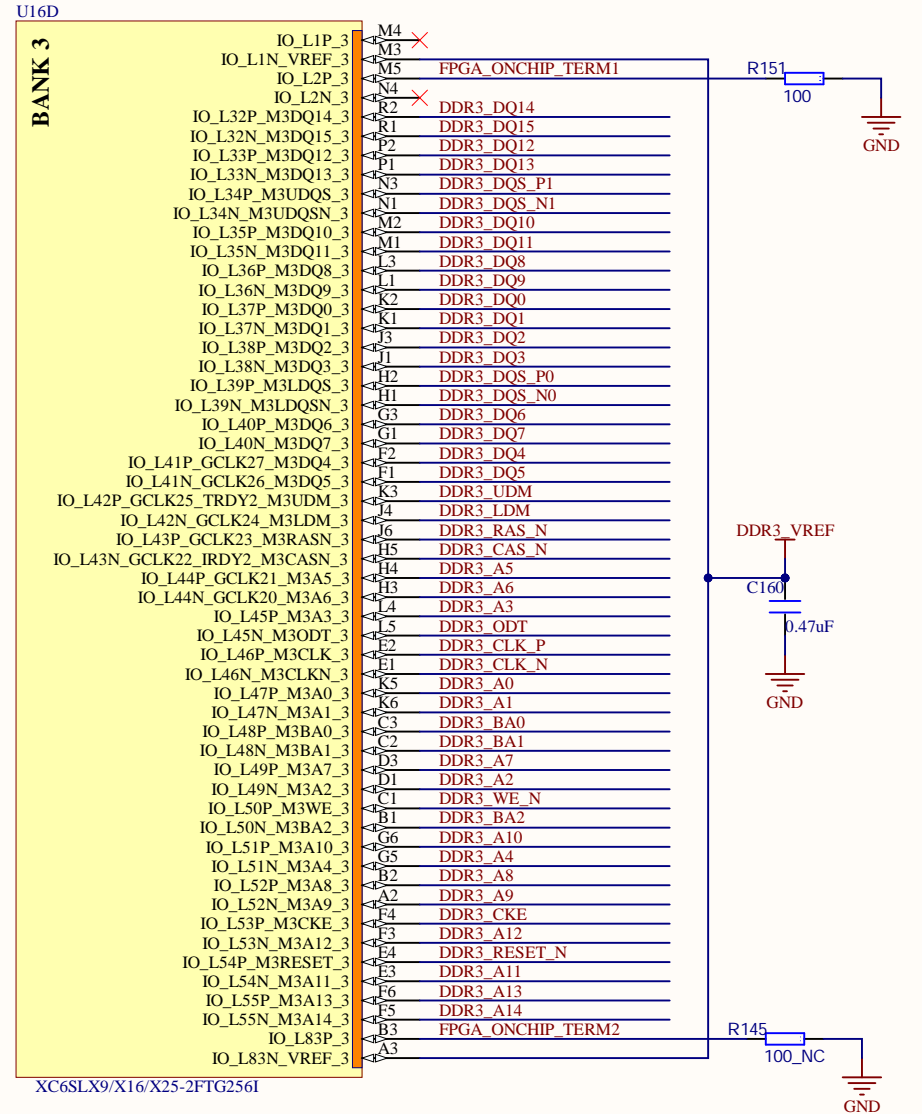
## QSPI FLASH



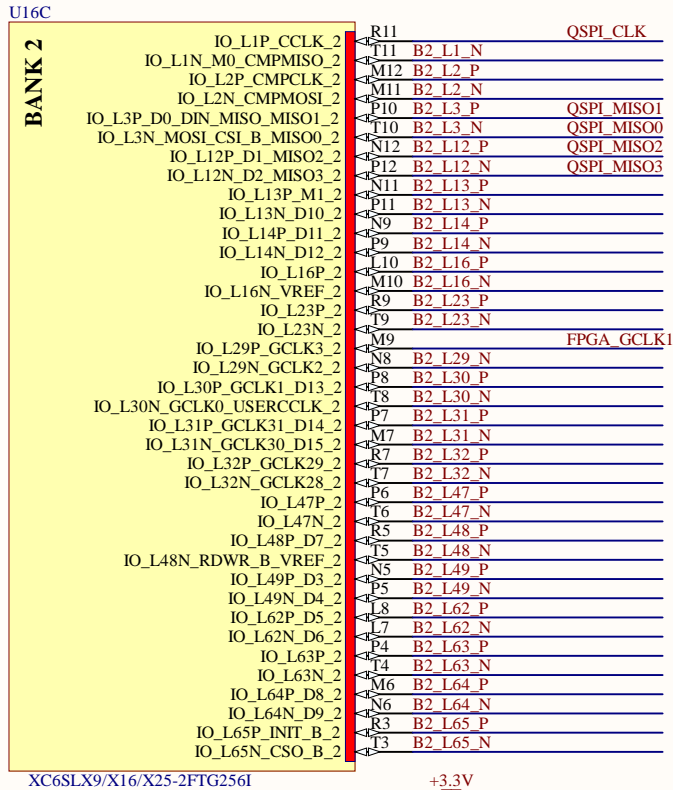
## XTAL



## FPGA BANK3

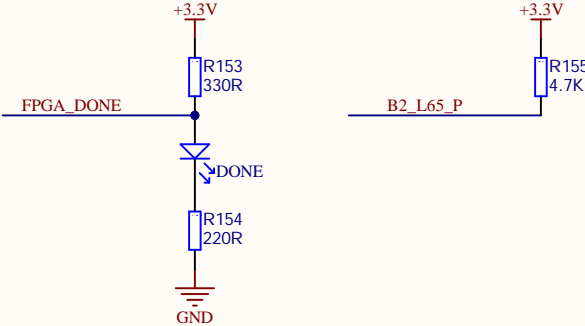
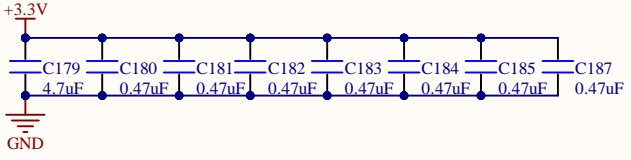
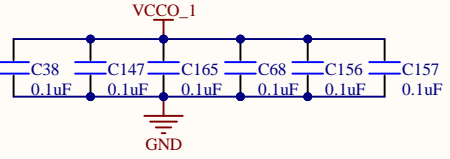
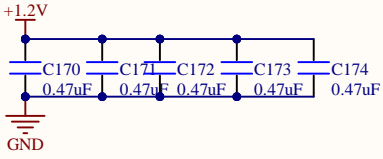
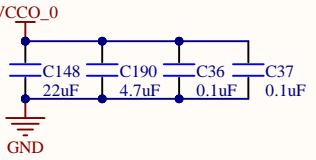
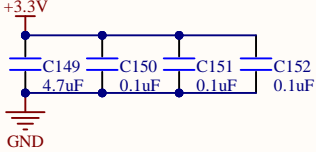
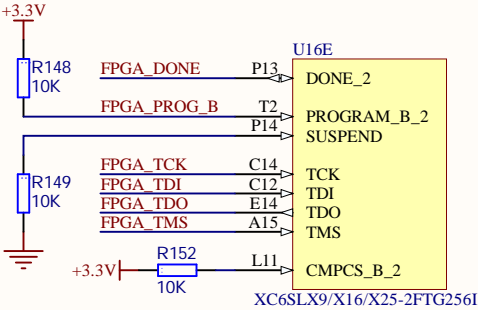
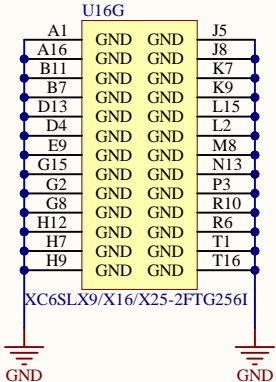
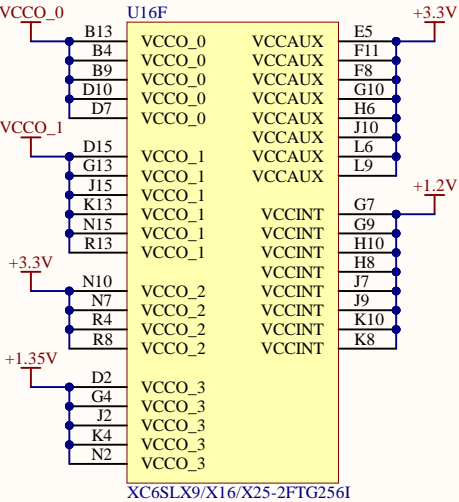


## FPGA BANK2

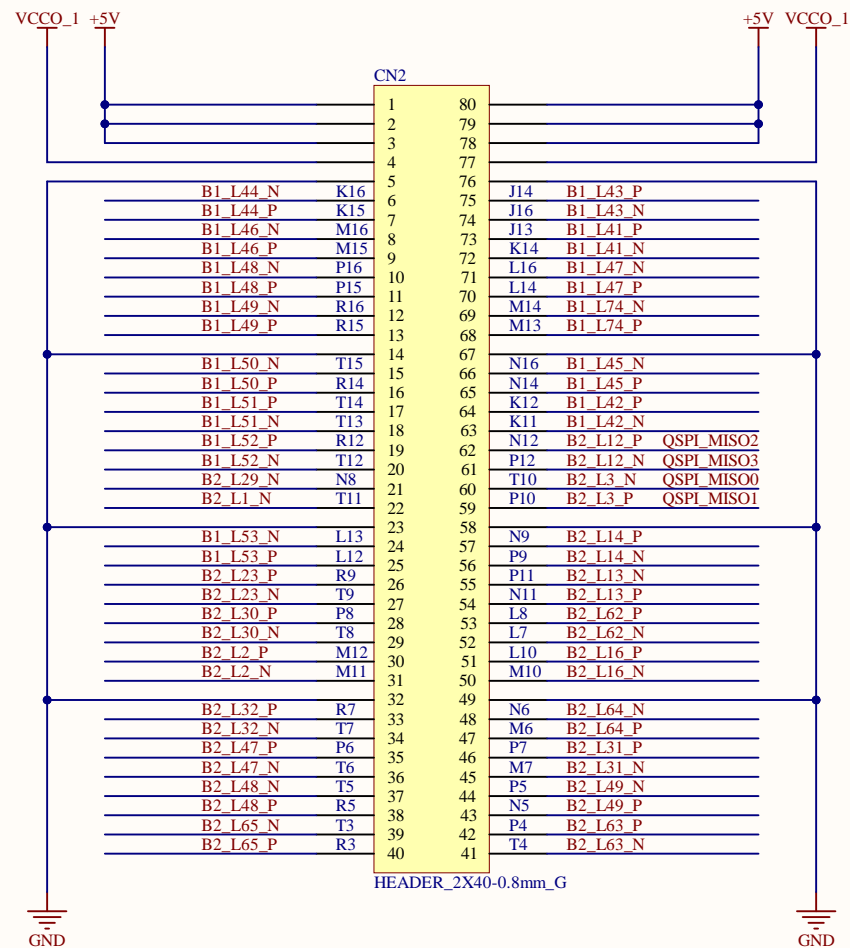
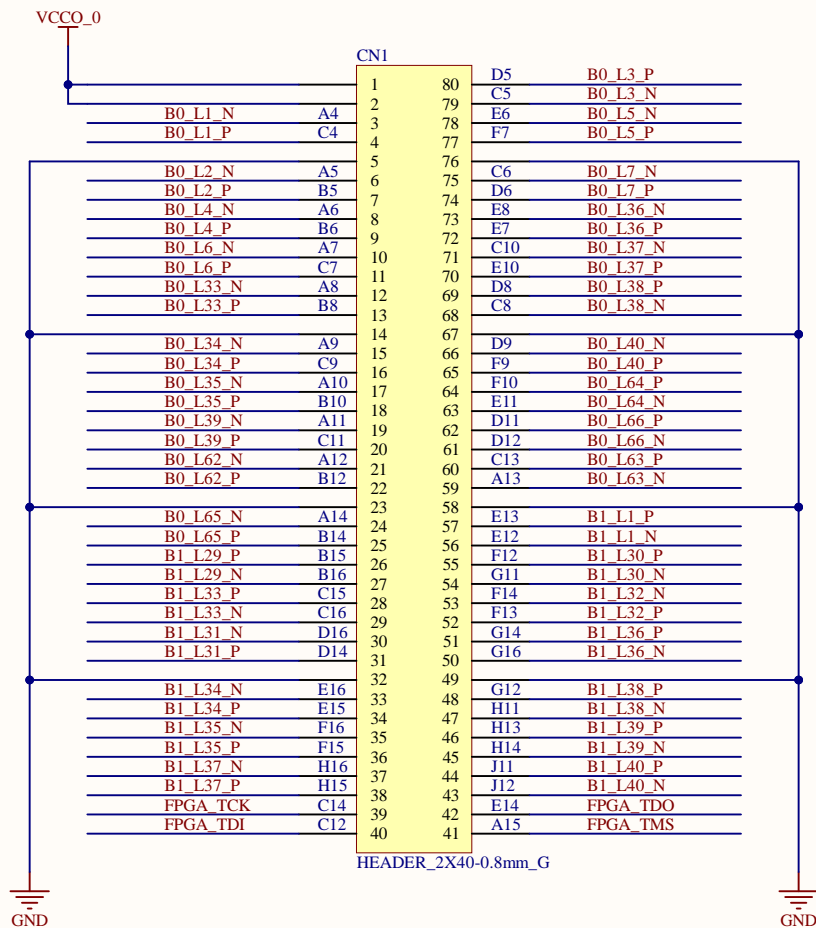


Title		
Size	Number	Revision
A4		
Date:	11/12/2024	Sheet of
File:	D:\01_rwl\03 FPGA_Bank2_Bank3.Sch	Drawn By:

FPGA POWER



Title		
Size	Number	Revision
A4		
Date:	11/12/2024	Sheet of
File:	D:\01_rw\...\04_FPGA_Power_Config.Sch	Drawn By:



Title

Size

A4

Number

Date: 11/12/2024

File: D:\01\_rw\...\05\_CONNECT.SchDoc

Revision

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